# 256-Position, One-Time Programmable, Dual-Channel, I²C® Digital Potentiometers

# AD5172/AD5173

## FEATURES

- 2-channel, 256-position potentiometers
- One-time programmable (OTP) set-and-forget resistance setting provides a low cost alternative to EEMEM
- Unlimited adjustments prior to OTP activation
- OTP overwrite allows dynamic adjustments with user-defined preset
- End-to-end resistance: 2.5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ
- Compact MSOP-10 (3 mm × 4.9 mm) package
- Fast settling time: $t_S$ = 5 µs typical in power-up
- Full read/write of wiper register
- Power-on preset to midscale
- Extra package address decode pins AD0 and AD1 (AD5173)
- Single supply: 2.7 V to 5.5 V
- Low temperature coefficient: 35 ppm/°C
- Low power: $I_{DD}$ = 6 µA maximum
- Wide operating temperature: −40°C to +125°C
- Software available for factory programming applications

## APPLICATIONS

- Systems calibration
- Electronics level setting
- Mechanical trimmers replacement in new designs
- Permanent factory PCB setting
- Transducer adjustment of pressure, temperature, position, chemical, and optical sensors
- RF amplifier biasing
- Automotive electronics adjustment
- Gain control and offset adjustment

## FUNCTIONAL BLOCK DIAGRAMS

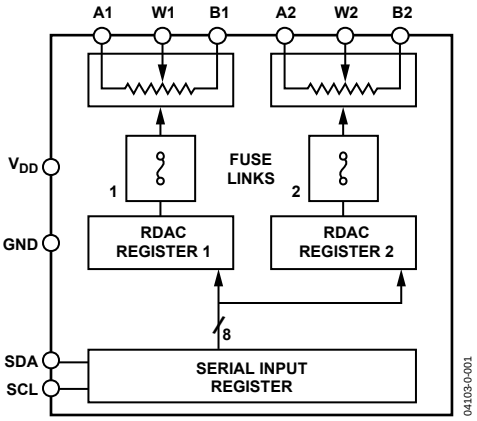


*Figure 1. AD5172 Functional Block Diagram*

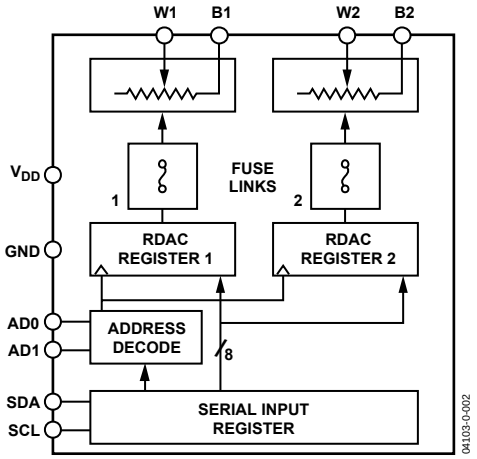


*Figure 2. AD5173 Functional Block Diagram*

## GENERAL OVERVIEW

The AD5172/AD5173 are dual-channel, 256-position, one-time programmable (OTP) digital potentiometers[1] that employ fuse link technology to achieve memory retention of resistance settings. OTP is a cost-effective alternative to EEMEM for users who do not need to program the digital potentiometer setting in memory more than once. These devices perform the same electronic adjustment function as mechanical potentiometers or variable resistors with enhanced resolution, solid-state reliability, and superior low temperature coefficient performance.

The AD5172/AD5173 are programmed using a 2-wire, I²C-compatible digital interface. Unlimited adjustments are allowed before permanently setting the resistance value. During OTP activation, a permanent blow fuse command freezes the wiper position (analogous to placing epoxy on a mechanical trimmer).

Unlike traditional OTP digital potentiometers, the AD5172/AD5173 have a unique temporary OTP overwrite feature that allows for new adjustments even after a fuse is blown. However, the OTP setting is restored during subsequent power-up conditions. This allows users to treat these digital potentiometers as volatile potentiometers with a programmable preset.

For applications that program the AD5172/AD5173 at the factory, Analog Devices offers device programming software running on Windows® 2000, Windows NT®, and Windows XP operating systems. This software effectively replaces any external I²C controllers, thus enhancing the time-to-market of the user's systems.

[1] The terms digital potentiometer, VR, and RDAC are used interchangeably.

**Rev. D**



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# ELECTRICAL CHARACTERISTICS—2.5 kΩ VERSION

$V_{DD}$ = 5 V ± 10% or 3 V ± 10%; $V_A = V_{DD}$; $V_B$ = 0 V; −40°C < $T_A$ < +125°C, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| DC CHARACTERISTICS—RHEOSTAT MODE | | | | | | |
| Resistor Differential Nonlinearity[2] | R-DNL | $R_{WB}$, $V_A$ = No connect | −2 | ±0.1 | +2 | LSB |
| Resistor Integral Nonlinearity[2] | R-INL | $R_{WB}$, $V_A$ = No connect | −6 | ±0.75 | +6 | LSB |
| Nominal Resistor Tolerance[3] | $\Delta R_{AB}$ | $T_A$ = 25°C | −20 | | +55 | % |
| Resistance Temperature Coefficient | $(\Delta R_{AB}/R_{AB})/\Delta T$ | | | 35 | | ppm/°C |
| RWB (Wiper Resistance) | $R_{WB}$ | Code = 0x00, $V_{DD}$ = 5 V | | 160 | 200 | Ω |
| DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (SPECIFICATIONS APPLY TO ALL VRs) | | | | | | |
| Differential Nonlinearity[4] | DNL | | −1.5 | ±0.1 | +1.5 | LSB |
| Integral Nonlinearity[4] | INL | | −2 | ±0.6 | +2 | LSB |
| Voltage Divider Temperature Coefficient | $(\Delta V_W/V_W)/\Delta T$ | Code = 0x80 | | 15 | | ppm/°C |
| Full-Scale Error | $V_{WFSE}$ | Code = 0xFF | −10 | −2.5 | 0 | LSB |
| Zero-Scale Error | $V_{WZSE}$ | Code = 0x00 | 0 | 2 | 10 | LSB |
| RESISTOR TERMINALS | | | | | | |
| Voltage Range[5] | $V_A$, $V_B$, $V_W$ | | GND | | $V_{DD}$ | V |
| Capacitance[6] A, B | $C_A$, $C_B$ | f = 1 MHz, measured to GND, code = 0x80 | | 45 | | pF |
| Capacitance[6] W | $C_W$ | f = 1 MHz, measured to GND, code = 0x80 | | 60 | | pF |
| Shutdown Supply Current[7] | $I_{A\_SD}$ | $V_{DD}$ = 5.5 V | | 0.01 | 1 | µA |
| Common-Mode Leakage | $I_{CM}$ | $V_A = V_B = V_{DD}/2$ | | 1 | | nA |
| DIGITAL INPUTS AND OUTPUTS | | | | | | |
| Input Logic High (SDA and SCL)[8] | $V_{IH}$ | $V_{DD}$ = 5 V | 0.7 $V_{DD}$ | | $V_{DD}$ + 0.5 | V |
| Input Logic Low (SDA and SCL)[8] | $V_{IL}$ | $V_{DD}$ = 5 V | −0.5 | | +0.3 $V_{DD}$ | V |
| Input Logic High (AD0 and AD1) | $V_{IH}$ | $V_{DD}$ = 3 V | 2.1 | | | V |
| Input Logic Low (AD0 and AD1) | $V_{IL}$ | $V_{DD}$ = 3 V | | | 0.6 | V |
| Input Current | $I_{IL}$ | $V_{IN}$ = 0 V or 5 V | | | ±1 | µA |
| Input Capacitance[6] | $C_{IL}$ | | | 5 | | pF |
| POWER SUPPLIES | | | | | | |
| Power Supply Range | $V_{DD\ RANGE}$ | | 2.7 | | 5.5 | V |
| OTP Supply Voltage[8, 9] | $V_{DD\_OTP}$ | $T_A$ = 25°C | 5.25 | | 5.5 | V |
| Supply Current | $I_{DD}$ | $V_{IH}$ = 5 V or $V_{IL}$ = 0 V | | 3.5 | 6 | µA |
| OTP Supply Current[8, 10] | $I_{DD\_OTP}$ | $V_{DD\_OTP}$ = 5.5 V, $T_A$ = 25°C | 100 | | | mA |
| Power Dissipation[11] | $P_{DISS}$ | $V_{IH}$ = 5 V or $V_{IL}$ = 0 V, $V_{DD}$ = 5 V | | | 30 | µW |
| Power Supply Sensitivity | PSS | $V_{DD}$ = 5 V ± 10%, code = midscale | | ±0.02 | ±0.08 | %/% |
| DYNAMIC CHARACTERISTICS[12] | | | | | | |
| Bandwidth −3 dB | BW_2.5K | Code = 0x80 | | 4.8 | | MHz |
| Total Harmonic Distortion | $THD_W$ | $V_A$ = 1 V rms, $V_B$ = 0 V, f = 1 kHz | | 0.1 | | % |
| $V_W$ Settling Time | $t_S$ | $V_A$ = 5 V, $V_B$ = 0 V, ±1 LSB error band | | 1 | | µs |
| Resistor Noise Voltage Density | $e_{N\_WB}$ | $R_{WB}$ = 1.25 kΩ, $R_S$ = 0 | | 3.2 | | nV/√Hz |

[1] Typical specifications represent average readings at 25°C and $V_{DD}$ = 5 V.
[2] Resistor position nonlinearity error, R-INL, is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. Parts are guaranteed monotonic.
[3] $V_{AB} = V_{DD}$, Wiper ($V_W$) = no connect.
[4] INL and DNL are measured at $V_W$ with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and $V_B$ = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminal A, Terminal B, and Terminal W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] Measured at the A terminal. The A terminal is open circuited in shutdown mode.
[8] The minimum voltage requirement on the $V_{IH}$ is 0.7 V × $V_{DD}$. For example, $V_{IH}$ min = 3.5 V when $V_{DD}$ = 5 V. It is typical for the SCL and SDA resistors to be pulled up to $V_{DD}$. However, care must be taken to ensure that the minimum $V_{IH}$ is met when the SCL and SDA are driven directly from a low voltage logic controller without pull-up resistors.
[9] Different from operating power supply; power supply for OTP is used one time only.
[10] Different from operating current; supply current for OTP lasts approximately 400 ms for one time only.
[11] $P_{DISS}$ is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[12] All dynamic characteristics use $V_{DD}$ = 5 V.

# ELECTRICAL CHARACTERISTICS—10 kΩ, 50 kΩ, 100 kΩ VERSIONS

$V_{DD}$ = 5 V ± 10% or 3 V ± 10%; $V_A = V_{DD}$; $V_B$ = 0 V; −40°C < $T_A$ < +125°C, unless otherwise noted.

**Table 2.**

| Parameter | Symbol | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| DC CHARACTERISTICS—RHEOSTAT MODE | | | | | | |
| Resistor Differential Nonlinearity[2] | R-DNL | $R_{WB}$, $V_A$ = No connect | −1 | ±0.1 | +1 | LSB |
| Resistor Integral Nonlinearity[2] | R-INL | $R_{WB}$, $V_A$ = No connect | −2.5 | ±0.25 | +2.5 | LSB |
| Nominal Resistor Tolerance[3] | $\Delta R_{AB}$ | $T_A$ = 25°C | −20 | | +20 | % |
| Resistance Temperature Coefficient | $(\Delta R_{AB}/R_{AB})/\Delta T$ | | | 35 | | ppm/°C |
| $R_{WB}$ (Wiper Resistance) | $R_{WB}$ | Code = 0x00, $V_{DD}$ = 5 V | | 160 | 200 | Ω |
| DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (SPECIFICATIONS APPLY TO ALL VRs) | | | | | | |
| Differential Nonlinearity[4] | DNL | | −1 | ±0.1 | +1 | LSB |
| Integral Nonlinearity[4] | INL | | −1 | ±0.3 | +1 | LSB |
| Voltage Divider Temperature Coefficient | $(\Delta V_W/V_W)/\Delta T$ | Code = 0x80 | | 15 | | ppm/°C |
| Full-Scale Error | $V_{WFSE}$ | Code = 0xFF | −2.5 | −1 | 0 | LSB |
| Zero-Scale Error | $V_{WZSE}$ | Code = 0x00 | 0 | 1 | 2.5 | LSB |
| RESISTOR TERMINALS | | | | | | |
| Voltage Range[5] | $V_A$, $V_B$, $V_W$ | | GND | | $V_{DD}$ | V |
| Capacitance[6] A, B | $C_A$, $C_B$ | f = 1 MHz, measured to GND, code = 0x80 | | 45 | | pF |
| Capacitance W[6] | $C_W$ | f = 1 MHz, measured to GND, code = 0x80 | | 60 | | pF |
| Shutdown Supply Current[7] | $I_{A\_SD}$ | $V_{DD}$ = 5.5 V | | 0.01 | 1 | µA |
| Common-Mode Leakage | $I_{CM}$ | $V_A = V_B = V_{DD}/2$ | | 1 | | nA |
| DIGITAL INPUTS AND OUTPUTS | | | | | | |
| Input Logic High (SDA and SCL)[8] | $V_{IH}$ | $V_{DD}$ = 5 V | 0.7 $V_{DD}$ | | $V_{DD}$ + 0.5 | V |
| Input Logic Low (SDA and SCL)[8] | $V_{IL}$ | $V_{DD}$ = 5 V | −0.5 | | +0.3 $V_{DD}$ | V |
| Input Logic High (AD0 and AD1) | $V_{IH}$ | $V_{DD}$ = 3 V | 2.1 | | | V |
| Input Logic Low (AD0 and AD1) | $V_{IL}$ | $V_{DD}$ = 3 V | | | 0.6 | V |
| Input Current | $I_{IL}$ | $V_{IN}$ = 0 V or 5 V | | | ±1 | µA |
| Input Capacitance[6] | $C_{IL}$ | | | 5 | | pF |
| POWER SUPPLIES | | | | | | |
| Power Supply Range | $V_{DD\ RANGE}$ | | 2.7 | | 5.5 | V |
| OTP Supply Voltage[8, 9] | $V_{DD\_OTP}$ | | 5.25 | | 5.5 | V |
| Supply Current | $I_{DD}$ | $V_{IH}$ = 5 V or $V_{IL}$ = 0 V | | 3.5 | 6 | µA |
| OTP Supply Current[8, 10] | $I_{DD\_OTP}$ | $V_{DD\_OTP}$ = 5.5 V, $T_A$ = 25°C | 100 | | | mA |
| Power Dissipation[11] | $P_{DISS}$ | $V_{IH}$ = 5 V or $V_{IL}$ = 0 V, $V_{DD}$ = 5 V | | | 30 | µW |
| Power Supply Sensitivity | PSS | $V_{DD}$ = +5 V ± 10%, code = midscale | | ±0.02 | ±0.08 | %/% |
| DYNAMIC CHARACTERISTICS[12] | | | | | | |
| Bandwidth −3 dB | BW | $R_{AB}$ = 10 kΩ, code = 0x80 | | 600 | | kHz |
| | | $R_{AB}$ = 50 kΩ, code = 0x80 | | 100 | | kHz |
| | | $R_{AB}$ = 100 kΩ, code = 0x80 | | 40 | | kHz |
| Total Harmonic Distortion | $THD_W$ | $V_A$ = 1 V rms, $V_B$ = 0 V, f = 1 kHz, $R_{AB}$ = 10 kΩ | | 0.1 | | % |
| $V_W$ Settling Time (10 kΩ/50 kΩ/100 kΩ) | $t_S$ | $V_A$ = 5 V, $V_B$ = 0 V, ±1 LSB error band | | 2 | | µs |
| Resistor Noise Voltage Density | $e_{N\_WB}$ | $R_{WB}$ = 5 kΩ, $R_S$ = 0 | | 9 | | nV/√Hz |

[1] Typical specifications represent average readings at 25°C and $V_{DD}$ = 5 V.
[2] Resistor position nonlinearity error, R-INL, is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. Parts are guaranteed monotonic.
[3] $V_{AB} = V_{DD}$, Wiper ($V_W$) = no connect.
[4] INL and DNL are measured at $V_W$ with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and $V_B$ = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminal A, Terminal B, and Terminal W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] Measured at the A terminal. The A terminal is open circuited in shutdown mode.
[8] The minimum voltage requirement on the $V_{IH}$ is 0.7 V × $V_{DD}$. For example, $V_{IH}$ min = 3.5 V when $V_{DD}$ = 5 V. It is typical for the SCL and SDA have resistors to be pulled up to $V_{DD}$. However, care must be taken to ensure that the minimum $V_{IH}$ is met when the SCL and SDA are driven directly from a low voltage logic controller without pull-up resistors.
[9] Different from operating power supply, power supply OTP is used one time only.
[10] Different from operating current, supply current for OTP lasts approximately 400 ms for one time only.
[11] $P_{DISS}$ is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[12] All dynamic characteristics use $V_{DD}$ = 5 V.

# TIMING CHARACTERISTICS—2.5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ VERSIONS

$V_{DD}$ = 5 V ± 10% or 3 V ± 10%; $V_A = V_{DD}$; $V_B$ = 0 V; −40°C < $T_A$ < +125°C, unless otherwise noted.

**Table 3.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| I²C INTERFACE TIMING CHARACTERISTICS[1] | | | | | | |
| SCL Clock Frequency | $f_{SCL}$ | | | | 400 | kHz |
| $t_{BUF}$ Bus Free Time Between Stop and Start | $t_1$ | | 1.3 | | | µs |
| $t_{HD;STA}$ Hold Time (Repeated Start) | $t_2$ | After this period, the first clock pulse is generated. | 0.6 | | | µs |
| $t_{LOW}$ Low Period of SCL Clock | $t_3$ | | 1.3 | | | µs |
| $t_{HIGH}$ High Period of SCL Clock | $t_4$ | | 0.6 | | | µs |
| $t_{SU;STA}$ Setup Time for Repeated Start Condition | $t_5$ | | 0.6 | | | µs |
| $t_{HD;DAT}$ Data Hold Time[2] | $t_6$ | | | | 0.9 | µs |
| $t_{SU;DAT}$ Data Setup Time | $t_7$ | | 100 | | | ns |
| $t_F$ Fall Time of Both SDA and SCL Signals | $t_8$ | | | | 300 | ns |
| $t_R$ Rise Time of Both SDA and SCL Signals | $t_9$ | | | | 300 | ns |
| $t_{SU;STO}$ Setup Time for Stop Condition | $t_{10}$ | | 0.6 | | | µs |

[1] See the timing diagrams for locations of measured values (see Figure 51 to Figure 55).
[2] The maximum $t_{HD;DAT}$ only has to be met if the device does not stretch the low period ($t_{LOW}$) of the SCL signal.

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 4.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to GND | −0.3 V to +7 V |
| $V_A$, $V_B$, $V_W$ to GND | $V_{DD}$ |
| Terminal Current, Ax to Bx, Ax to Wx, Bx to Wx[1] | |
| Pulsed | ±20 mA |
| Continuous | ±5 mA |
| Digital Inputs and Output Voltage to GND | 0 V to 7 V |
| Operating Temperature Range | −40°C to +125°C |
| Maximum Junction Temperature ($T_{JMAX}$) | 150°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |
| Thermal Resistance[2] | |
| $\theta_{JA}$: MSOP-10 | 230°C/W |

[1] Maximum terminal current is bound by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
[2] Package power dissipation = ($T_J$ max − $T_A$)/$\theta_{JA}$.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

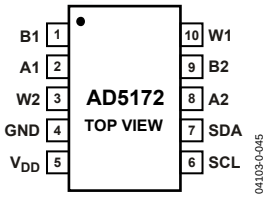



*Figure 3. AD5172 Pin Configuration*

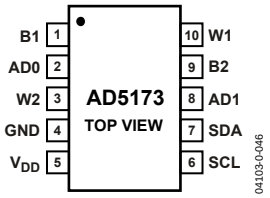



*Figure 4. AD5173 Pin Configuration*

**Table 5. AD5172 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | B1 | B1 Terminal. GND ≤ $V_{B1}$ ≤ $V_{DD}$. |
| 2 | A1 | A1 Terminal. GND ≤ $V_{A1}$ ≤ $V_{DD}$. |
| 3 | W2 | W2 Terminal. GND ≤ $V_{W2}$ ≤ $V_{DD}$. |
| 4 | GND | Digital Ground. |
| 5 | $V_{DD}$ | Positive Power Supply. Specified for operation from 2.7 V to 5.5 V. For OTP programming, $V_{DD}$ needs to be a minimum of 5.25 V but no more than 5.5 V and have a 100 mA driving capability. |
| 6 | SCL | Serial Clock Input. Positive-edge triggered. Requires a pull-up resistor. If it is driven direct from a logic controller without the pull-up resistor, ensure that $V_{IH}$ min is 0.7 V × $V_{DD}$. |
| 7 | SDA | Serial Data Input/Output. Requires a pull-up resistor. If it is driven direct from a logic controller without the pull-up resistor, ensure that $V_{IH}$ min is 0.7 V × $V_{DD}$. |
| 8 | A2 | A2 Terminal. GND ≤ $V_{A2}$ ≤ $V_{DD}$. |
| 9 | B2 | B2 Terminal. GND ≤ $V_{B2}$ ≤ $V_{DD}$. |
| 10 | W1 | W1 Terminal. GND ≤ $V_{W1}$ ≤ $V_{DD}$. |

**Table 6. AD5173 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | B1 | B1 Terminal. GND ≤ $V_{B1}$ ≤ $V_{DD}$. |
| 2 | AD0 | Programmable Address Bit 0 for Multiple Package Decoding. |
| 3 | W2 | W2 Terminal. GND ≤ $V_{W2}$ ≤ $V_{DD}$. |
| 4 | GND | Digital Ground. |
| 5 | $V_{DD}$ | Positive Power Supply. Specified for operation from 2.7 V to 5.5 V. For OTP programming, $V_{DD}$ needs to be a minimum of 5.25 V but no more than 5.5 V and have a 100 mA driving capability. |
| 6 | SCL | Serial Clock Input. Positive-edge triggered. Requires a pull-up resistor. If it is driven direct from a logic controller without the pull-up resistor, ensure that $V_{IH}$ min is 0.7 V × $V_{DD}$. |
| 7 | SDA | Serial Data Input/Output. Requires a pull-up resistor. If it is driven direct from a logic controller without the pull-up resistor, ensure that $V_{IH}$ min is 0.7 V × $V_{DD}$. |
| 8 | AD1 | Programmable Address Bit 1 for Multiple Package Decoding. |
| 9 | B2 | B2 Terminal. GND ≤ $V_{B2}$ ≤ $V_{DD}$. |
| 10 | W1 | W1 Terminal. GND ≤ $V_{W1}$ ≤ $V_{DD}$. |

# TYPICAL PERFORMANCE CHARACTERISTICS

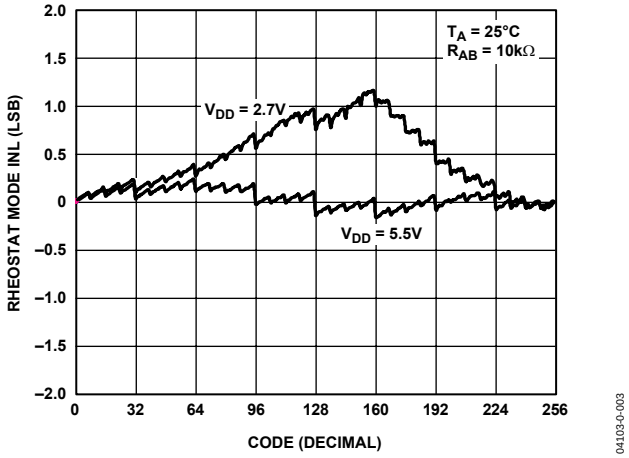



Figure 5. R-INL vs. Code vs. Supply Voltages

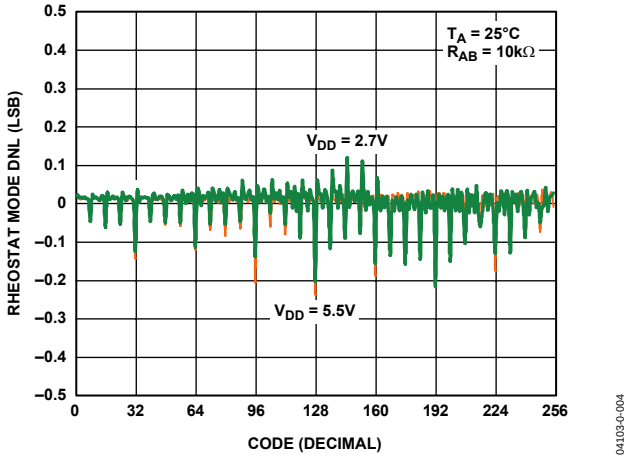



Figure 6. R-DNL vs. Code vs. Supply Voltages

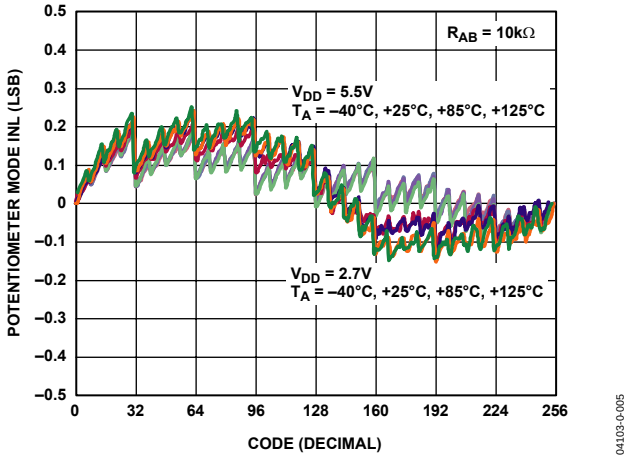



Figure 7. INL vs. Code vs. Temperature

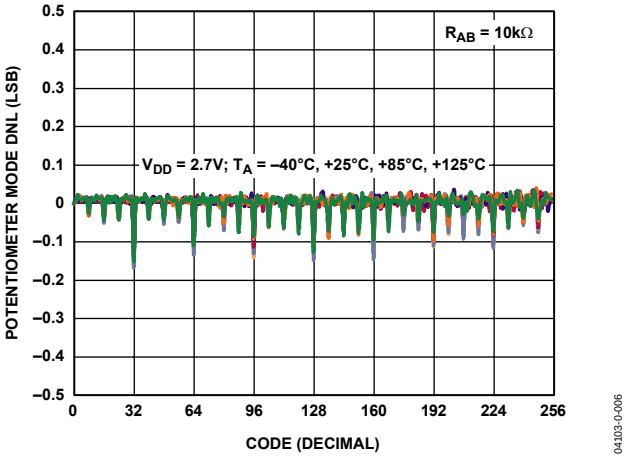



Figure 8. DNL vs. Code vs. Temperature

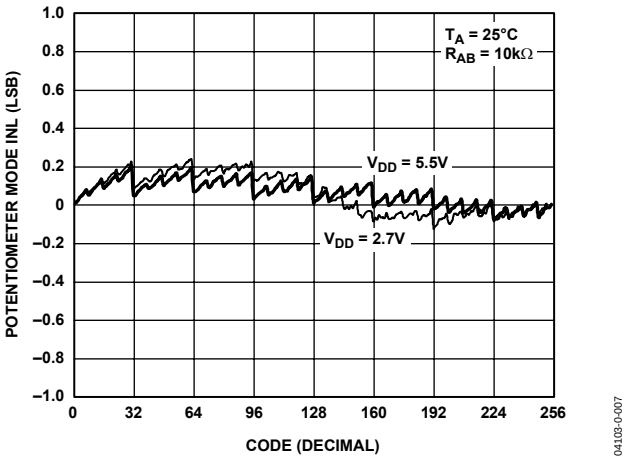



Figure 9. INL vs. Code vs. Supply Voltages

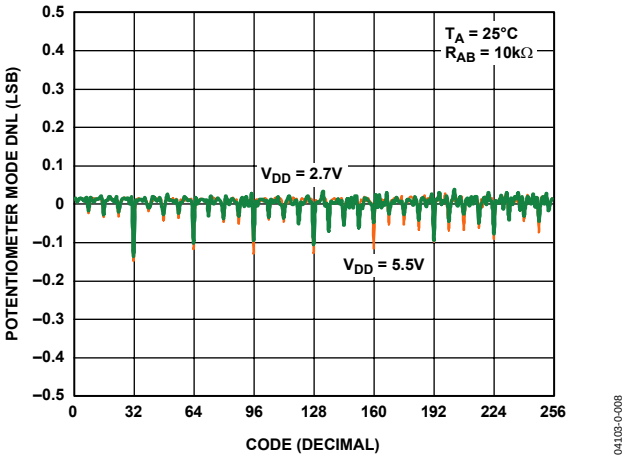



Figure 10. DNL vs. Code vs. Supply Voltages

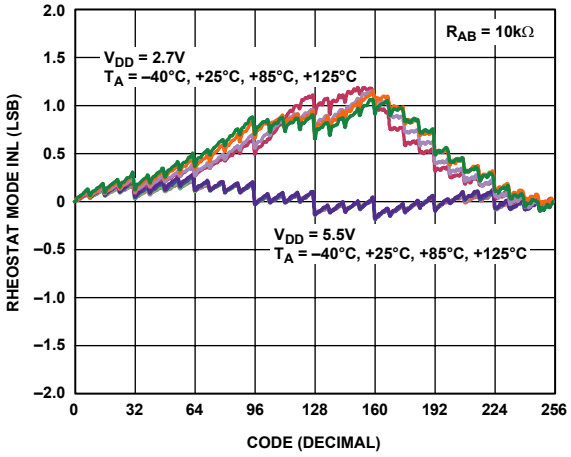



Figure 11. R-INL vs. Code vs. Temperature

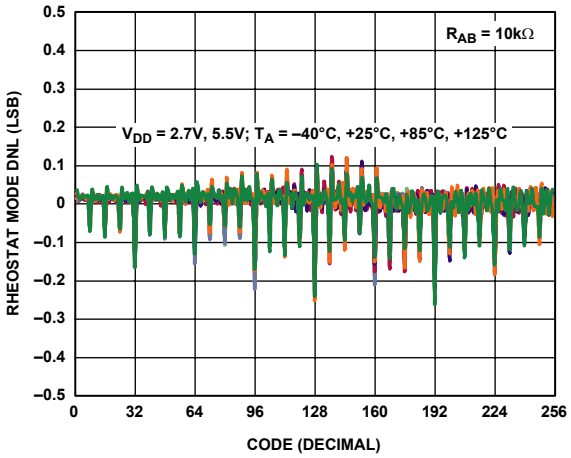



Figure 12. R-DNL vs. Code vs. Temperature

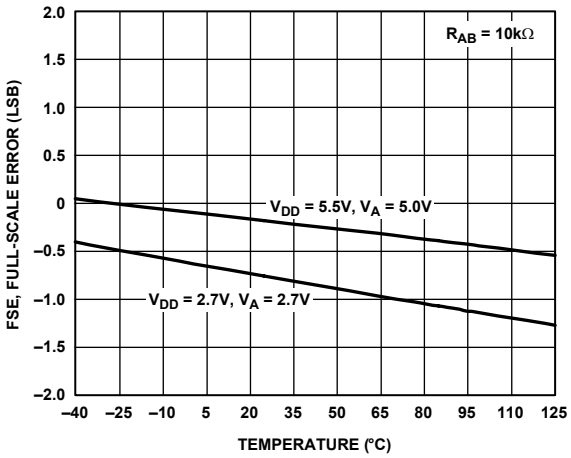



Figure 13. Full-Scale Error vs. Temperature

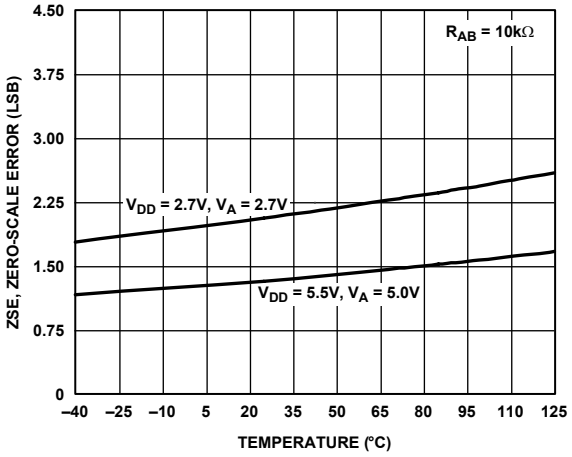



Figure 14. Zero-Scale Error vs. Temperature

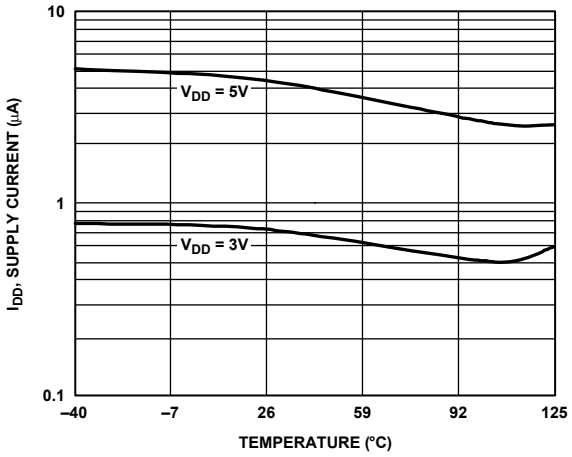



Figure 15. Supply Current vs. Temperature

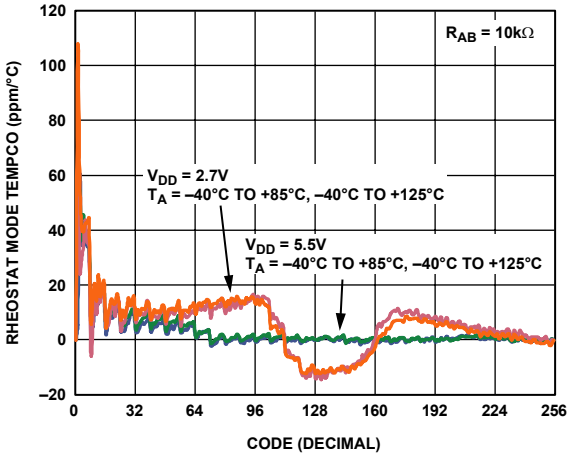



Figure 16. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

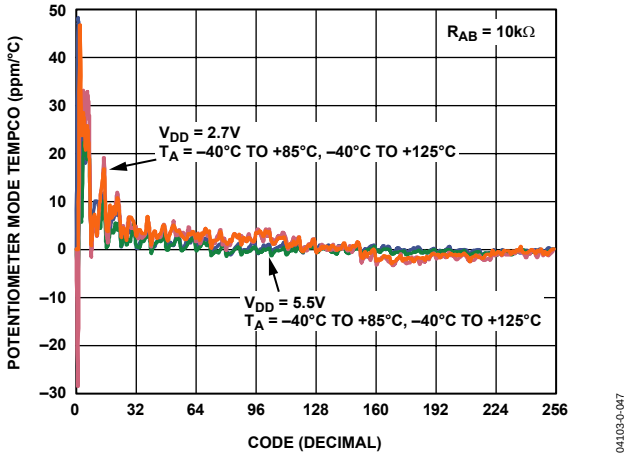



Figure 17. AD5172 Potentiometer Mode Tempco $\Delta V_{WB}/\Delta T$ vs. Code

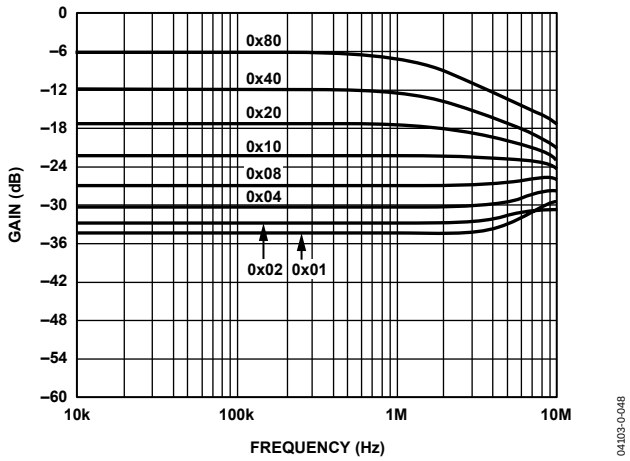



Figure 18. Gain vs. Frequency vs. Code, $R_{AB}$ = 2.5 kΩ

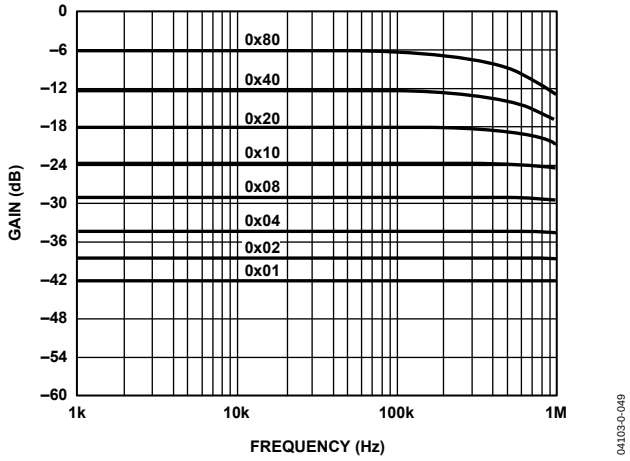



Figure 19. Gain vs. Frequency vs. Code, $R_{AB}$ = 10 kΩ

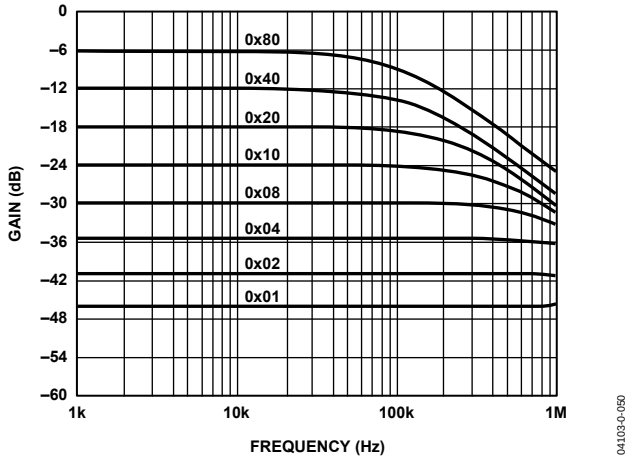



Figure 20. Gain vs. Frequency vs. Code, $R_{AB}$ = 50 kΩ

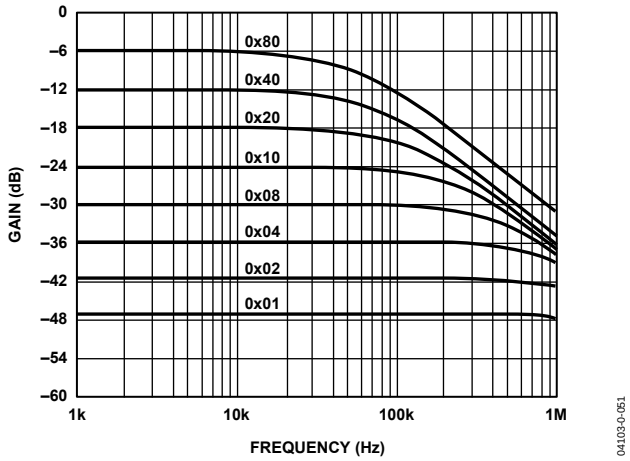



Figure 21. Gain vs. Frequency vs. Code, $R_{AB}$ = 100 kΩ

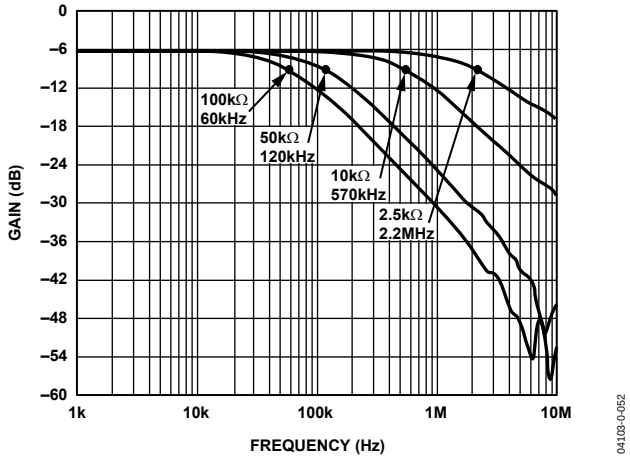



Figure 22. –3 dB Bandwidth @ Code = 0x80

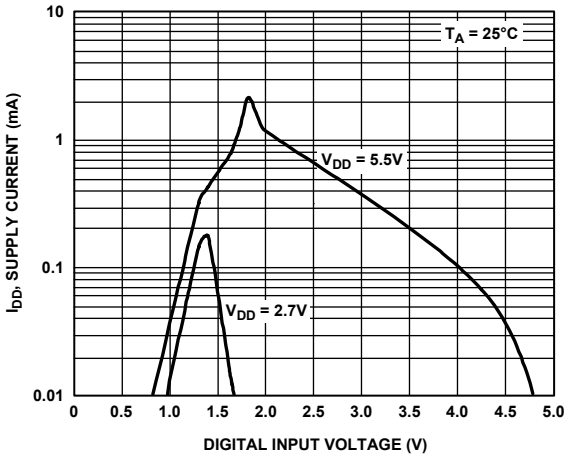



*Figure 23. $I_{DD}$ vs. Input Voltage*

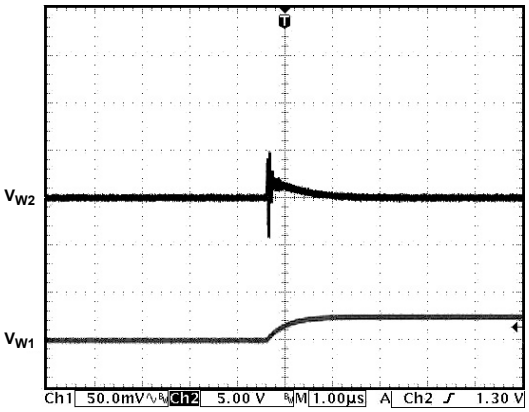



*Figure 26. Analog Crosstalk*

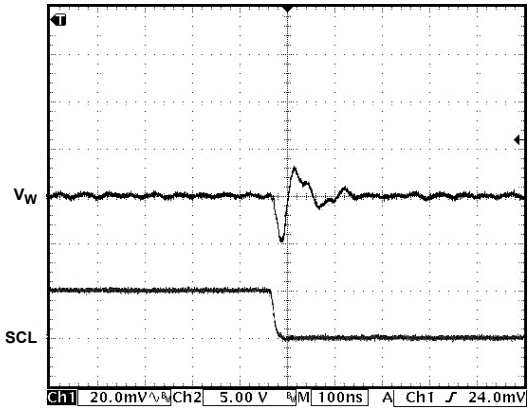



*Figure 24. Digital Feedthrough*

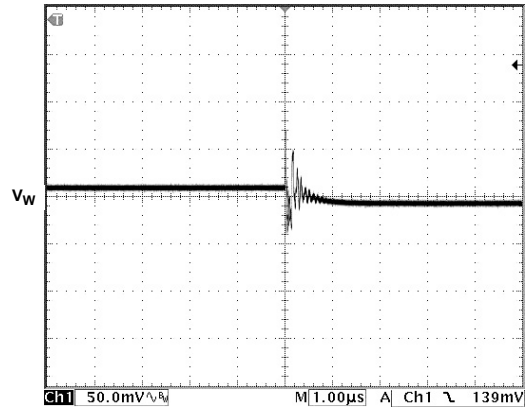



*Figure 27. Midscale Glitch, Code 0x80 to Code 0x7F*

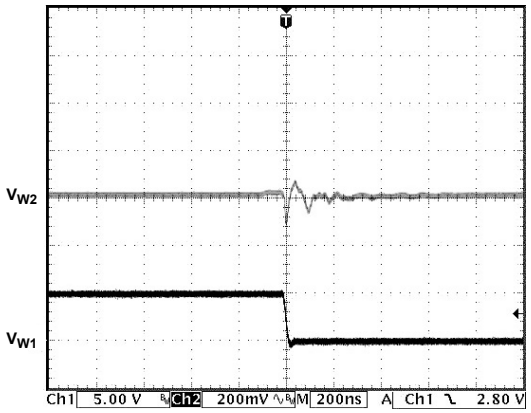



*Figure 25. Digital Crosstalk*

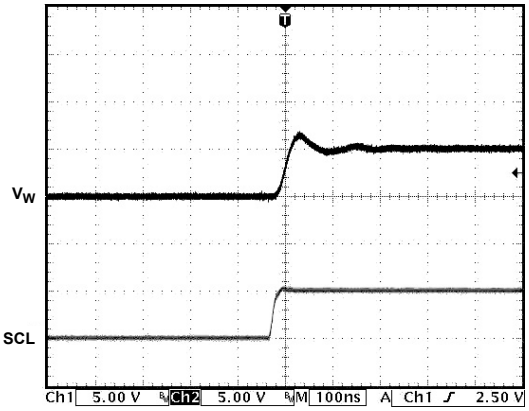



*Figure 28. Large Signal Settling Time*

# TEST CIRCUITS

Figure 29 to Figure 36 illustrate the test circuits that define the test conditions used in the product specification tables.

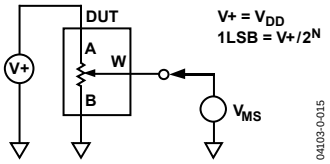



Figure 29. Potentiometer Divider Nonlinearity Error (INL, DNL)

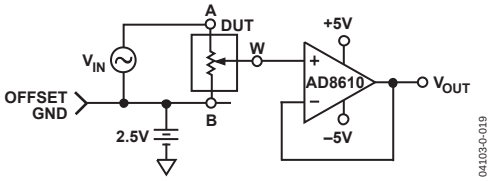



Figure 33. Test Circuit for Gain vs. Frequency

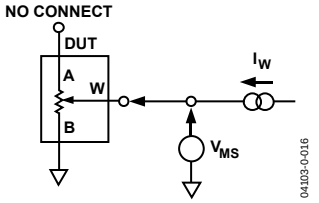



Figure 30. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

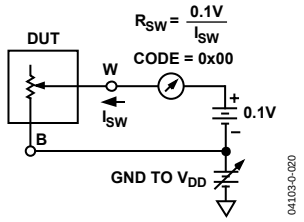



Figure 34. Incremental On Resistance

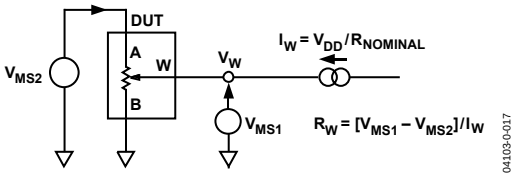



Figure 31. Wiper Resistance

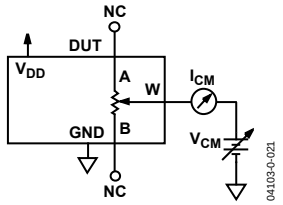



Figure 35. Common-Mode Leakage Current

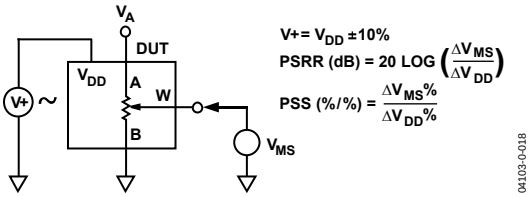



Figure 32. Power Supply Sensitivity (PSS, PSSR)

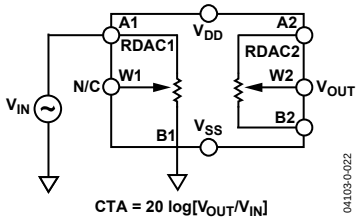



Figure 36. Analog Crosstalk

# THEORY OF OPERATION

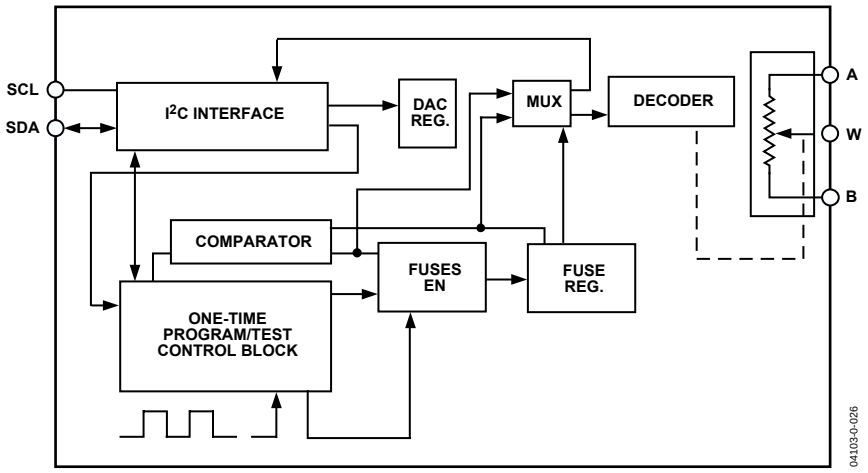



*Figure 37. Detailed Functional Block Diagram*

The AD5172/AD5173 are 256-position, digitally controlled variable resistors (VRs) that employ fuse link technology to achieve memory retention of resistance setting.

An internal power-on preset places the wiper at midscale during power-on. If the OTP function is activated, the device powers up at the user-defined permanent setting.

## ONE-TIME PROGRAMMING (OTP)

Prior to OTP activation, the AD5172/AD5173 presets to mid-scale during initial power-on. After the wiper is set to the desired position, the resistance can be permanently set by programming the T bit high, the proper coding (see Table 7 and Table 8), and one-time $V_{DD\_OTP}$. The fuse link technology of the AD517x family of digital potentiometers requires $V_{DD\_OTP}$ to be between 5.25 V and 5.5 V to blow the fuses to achieve a given nonvolatile setting. Conversely, $V_{DD}$ can be 2.7 V to 5.5 V during operation. As a result, system supply that is lower than 5.25 V requires an external supply for one-time programming. The user is allowed only one attempt to blow the fuses. If the user fails to blow the fuses during this attempt, the structure of the fuses can change such that they may never be blown, regardless of the energy applied at subsequent events. For details, see the Power Supply Considerations section.

The device control circuit has two validation bits, E1 and E0, that can be read back to check the programming status (see Table 10). Users should always read back the validation bits to ensure that the fuses are properly blown. After the fuses are blown, all fuse latches are enabled upon subsequent power-on; therefore, the output corresponds to the stored setting. Figure 37 shows a detailed functional block diagram.

## PROGRAMMING THE VARIABLE RESISTOR AND VOLTAGE

### *Rheostat Operation*

The nominal resistance of the RDAC between Terminal A and Terminal B is available in 2.5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ. The nominal resistance ($R_{AB}$) of the VR has 256 contact points accessed by the wiper terminal and the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings.

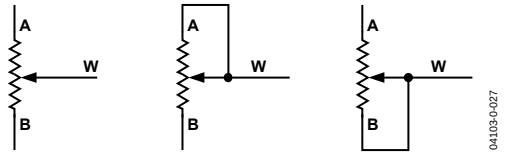



*Figure 38. Rheostat Mode Configuration*

Assuming a 10 kΩ part is used, the wiper's first connection starts at the B terminal for Data 0x00. Because there is a 50 Ω wiper contact resistance, such a connection yields a minimum of 100 Ω (2 × 50 Ω) resistance between Terminal W and Terminal B. The second connection is the first tap point, which corresponds to 139 Ω ($R_{WB} = R_{AB}/256 + 2 \times R_W = 39\ \Omega + 2 \times 50\ \Omega$) for Data 0x01. The third connection is the next tap point, representing 178 Ω (2 × 39 Ω + 2 × 50 Ω) for Data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10100 Ω ($R_{AB} + 2 \times R_W$).

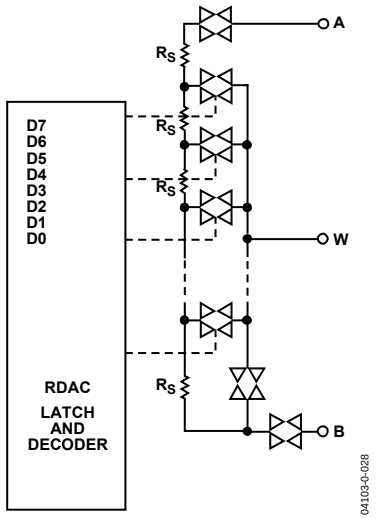



*Figure 39. AD5172/AD5173 Equivalent RDAC Circuit*

The general equation that determines the digitally programmed output resistance between W and B is

$$R_{WB}(D) = \frac{D}{128} \times R_{AB} + 2 \times R_W \quad (1)$$

where:

$D$ is the decimal equivalent of the binary code loaded in the 8-bit RDAC register.

$R_{AB}$ is the end-to-end resistance.

$R_W$ is the wiper resistance contributed by the on resistance of the internal switch.

In summary, if $R_{AB}$ = 10 kΩ and the A terminal is open circuited, the output resistance $R_{WB}$ is set for the RDAC latch codes, as shown in Table 7.

**Table 7. Codes and Corresponding $R_{WB}$ Resistance**

| D (Dec) | $R_{WB}$ (Ω) | Output State |
|---|---|---|
| 255 | 9961 | Full scale ($R_{AB}$ – 1 LSB + $R_W$) |
| 128 | 5060 | Midscale |
| 1 | 139 | 1 LSB |
| 0 | 100 | Zero scale (wiper contact resistance) |

Note that in the zero-scale condition, a finite wiper resistance of 100 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the Wiper W and Terminal A also produces a digitally controlled complementary resistance, $R_{WA}$. When these terminals are used, the B terminal can be opened. Setting the resistance value for $R_{WA}$ starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value.

The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{128} \times R_{AB} + 2 \times R_W \quad (2)$$

For $R_{AB}$ = 10 kΩ and the B terminal open circuited, the following output resistance $R_{WA}$ is set for the RDAC latch codes, as shown in Table 8.

**Table 8. Codes and Corresponding $R_{WA}$ Resistance**

| D (Dec) | $R_{WA}$ (Ω) | Output State |
|---|---|---|
| 255 | 139 | Full scale |
| 128 | 5060 | Midscale |
| 1 | 9961 | 1 LSB |
| 0 | 10060 | Zero scale |

Typical device-to-device matching is process-lot dependent and can vary up to ±30%. Because the resistance element is processed using thin film technology, the change in $R_{AB}$ with temperature has a very low 35 ppm/°C temperature coefficient.

## PROGRAMMING THE POTENTIOMETER DIVIDER

### *Voltage Output Operation*

The digital potentiometer easily generates a voltage divider at wiper to B and wiper to A proportional to the input voltage at A to B. Unlike the polarity of $V_{DD}$ to GND, which must be positive, voltage across A to B, W to A, and W to B can be at either polarity.

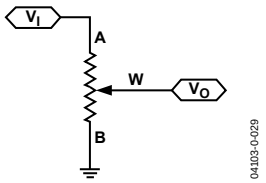



*Figure 40. Potentiometer Mode Configuration*

If ignoring the effect of the wiper resistance for approximation, connecting the A terminal to 5 V and the B terminal to ground produces an output voltage at the wiper to B starting at 0 V up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across Terminal A and Terminal B divided by the 256 positions of the potentiometer divider. The general equation defining the output voltage at $V_W$ with respect to ground for any valid input voltage applied to Terminal A and Terminal B is

$$V_W(D) = \frac{D}{256} V_A + \frac{256 - D}{256} V_B \quad (3)$$

For a more accurate calculation, which includes the effect of wiper resistance, $V_W$ can be found as

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} V_A + \frac{R_{WA}(D)}{R_{AB}} V_B \quad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors $R_{WA}$ and $R_{WB}$ and not the absolute values. Thus, the temperature drift reduces to 15 ppm/°C.

## ESD PROTECTION

All digital inputs, SDA, SCL, AD0, and AD1, are protected with a series input resistor and parallel Zener ESD structures, as shown in Figure 41 and Figure 42.

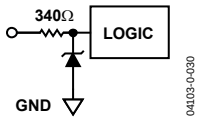



*Figure 41. ESD Protection of Digital Pins*

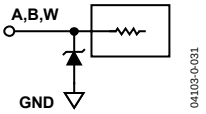



*Figure 42. ESD Protection of Resistor Terminals*

## TERMINAL VOLTAGE OPERATING RANGE

The AD5172/AD5173 $V_{DD}$ to GND power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on Terminal A, Terminal B, and Terminal W that exceed $V_{DD}$ or GND are clamped by the internal forward-biased diodes (see Figure 43).

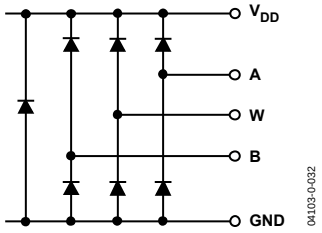



*Figure 43. Maximum Terminal Voltages Set by $V_{DD}$ and GND*

## POWER-UP SEQUENCE

Because the ESD protection diodes limit the voltage compliance at Terminal A, Terminal B, and Terminal W (see Figure 43), it is important to power $V_{DD}$/GND before applying any voltage to Terminal A, Terminal B, and Terminal W. Otherwise, the diode is forward biased such that $V_{DD}$ is powered unintentionally and can affect the rest of the user's circuit. The ideal power-up sequence is GND, $V_{DD}$, the digital inputs, and then $V_A$/$V_B$/$V_W$. The relative order of powering $V_A$, $V_B$, $V_W$, and the digital inputs is not important as long as they are powered after $V_{DD}$/GND.

## POWER SUPPLY CONSIDERATIONS

To minimize the package pin count, both the one-time programming and normal operating voltage supplies are applied to the same $V_{DD}$ terminal of the device. The AD5172/AD5173 employ fuse link technology that requires 5.25 V to 5.5 V to blow the internal fuses to achieve a given setting, but normal $V_{DD}$ can be 2.7 V to 5.5 V. Such dual-voltage requirements need isolation between the supplies if $V_{DD}$ is lower than the required $V_{DD\_OTP}$. The fuse programming supply (either an on-board regulator or rack-mount power supply) must be rated at 5.25 V to 5.5 V and must be able to provide a 100 mA transient current for 400 ms for successful one-time programming. Once programming is completed, the $V_{DD\_OTP}$ supply must be removed to allow normal operation at 2.7 V to 5.5 V, and the device consumes only microamps of current. Figure 44 shows the simplest implementation to meet the dual-voltage requirement with a jumper. This approach saves one voltage supply but draws additional current and requires manual configuration.

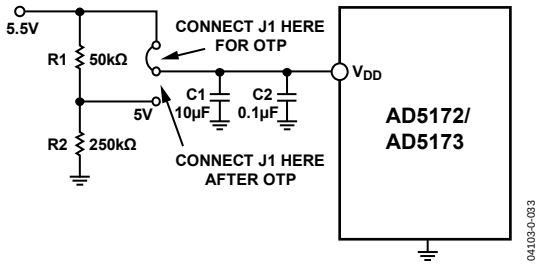



*Figure 44. Power Supply Requirements*

An alternate approach in 3.5 V to 5.25 V systems adds a signal diode between the system supply and the OTP supply for isolation, as shown in Figure 45. The $V_{DD\_OTP}$ supply must be removed once OTP is completed.

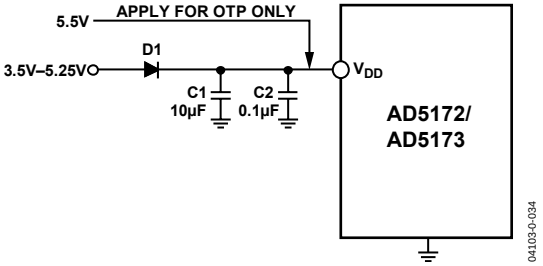



*Figure 45. Isolate 5.5 V OTP Supply from 3.5 V to 5.25 V Normal Operating Supply*

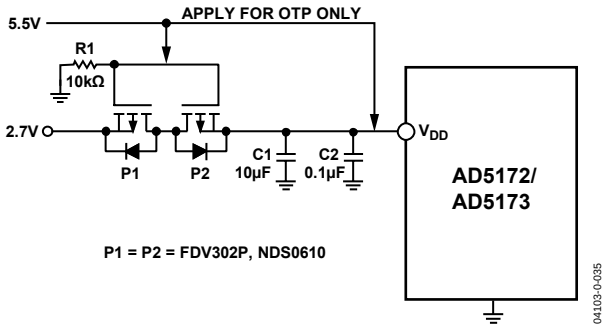



*Figure 46. Isolate 5.5 V OTP Supply from 2.7 V Normal Operating Supply*

For users who operate their systems at 2.7 V, use of the bidirectional, low threshold P-channel MOSFETs is recommended for the supply's isolation. As shown in Figure 46, this assumes that the 2.7 V system voltage is applied first, and that the P1 and P2 gates are pulled to ground, thus turning on P1 and subsequently P2. As a result, $V_{DD}$ of the AD5172/AD5173 approaches 2.7 V. When the AD5172/AD5173 setting is found, the factory tester applies the $V_{DD\_OTP}$ to both the $V_{DD}$ and the MOSFET gates, thus turning P1 and P2 off. The OTP command should be executed at this time to program the AD5172/AD5173 while the 2.7 V source is protected. Once the OTP is completed, the tester withdraws the $V_{DD\_OTP}$ and the AD5172/AD5173's setting is fixed permanently.

The AD5172/AD5173 achieve the OTP function by blowing internal fuses. Users should always apply the 5.25 V to 5.5 V one-time program voltage requirement at the first fuse programming attempt. Failure to comply with this requirement can lead to the change of fuse structures, rendering programming inoperable.

Care should be taken when SCL and SDA are driven from a low voltage logic controller. Users must ensure that the logic high level is between 0.7 V × $V_{DD}$ and $V_{DD}$ + 0.5 V.

Poor PCB layout introduces parasitics that can affect fuse programming. Therefore, it is recommended to add a 1 µF to 10 µF tantalum capacitor in parallel with a 1 nF ceramic capacitor as close as possible to the $V_{DD}$ pin. The type and value chosen for both capacitors are important. These capacitors work together to provide both a fast response and large supply current handling with minimum supply droop during transients. As a result, these capacitors increase the OTP programming success by not inhibiting the proper energy needed to blow the internal fuses. Additionally, C1 minimizes transient disturbance and low frequency ripple, while C2 reduces high frequency noise during normal operation.

## LAYOUT CONSIDERATIONS

In PCB layout, it is a good practice to employ compact, minimum lead length design. The leads to the inputs should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Note that the digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.

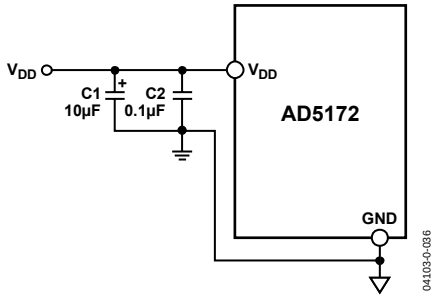



*Figure 47. Power Supply Bypassing*

# DEVICE PROGRAMMING SOFTWARE

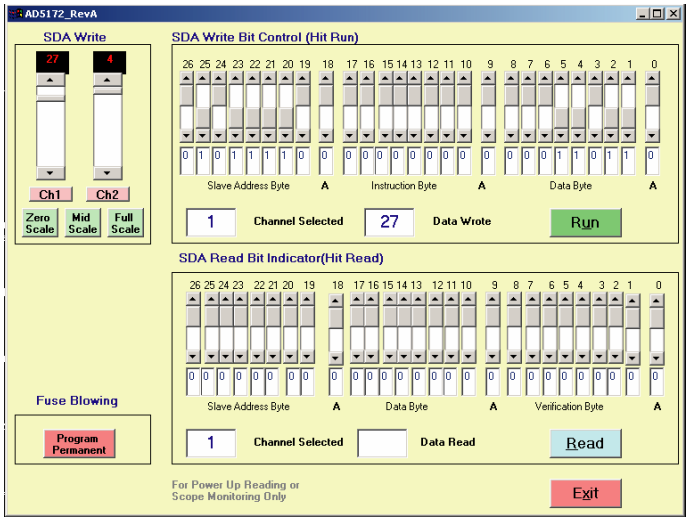



*Figure 48. AD5172/AD5173 Computer Software Interface*

Due to the advantages of the one-time programmable feature, consider programming the device in the factory before shipping the final product to end users. ADI offers device programming software that can be implemented in the factory on PCs running Windows 95 or later. As a result, external controllers are not required, which significantly reduces development time. The program is an executable file that does not require knowledge of programming languages or programming skills, and it is easy to set up and use. Figure 48 shows the software interface. The software can be downloaded at: www.analog.com/en/content/0,2886,761%255F797%255F29054,00.html.

The AD5172/AD5173 start at midscale after power-up, prior to OTP programming. To increment or decrement the resistance, move the scrollbars on the left. To write any specific value, use the bit pattern in the upper screen and click **Run**. The format of writing data to the device is shown in Table 9. Once the desired setting is found, click **Program Permanent** to blow the internal fuse links.

To read the validation bits and data out from the device, click **Read**. The format of the read bits is shown in Table 10.

To apply the device programming software in the factory, users must modify a 25-pin parallel port cable and configure Pin 2, Pin 3, Pin 15, and Pin 25 for SDA_write, SCL, SDA_read, and DGND, respectively, for the control signals (see Figure 49). Users should also layout the PCB of the AD5172/AD5173 as shown in Figure 50. The SCL and SDA pads allow pogo pins to be inserted so that signals can be communicated through the parallel port for the programming.

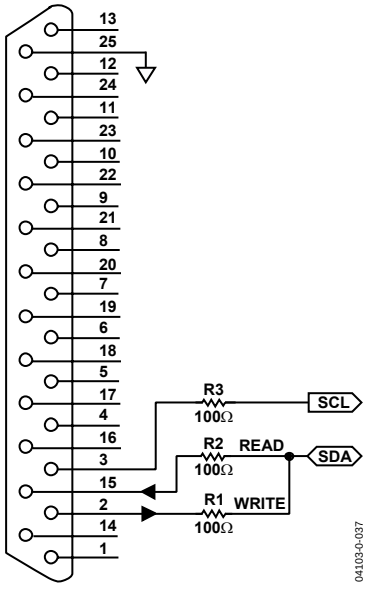



*Figure 49. Parallel Port Connection*
*(Pin 2 = SDA_write, Pin 3 = SCL, Pin 15 = SDA_read, and Pin 25 = DGND)*

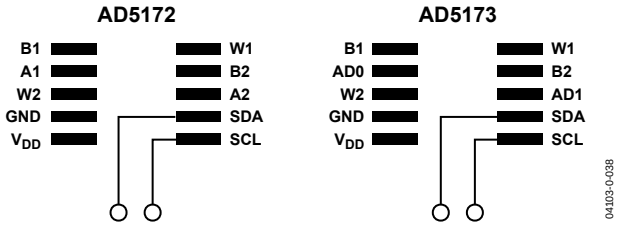



*Figure 50. Recommended AD5172/AD5173 PCB Layout*

# I²C INTERFACE

Table 9 and Table 10 use the following codes:

S = Start condition.

P = Stop condition.

A = Acknowledge.

AD0, AD1 = Package pin programmable address bits.

X = Don't care.

$\overline{W}$ = Write.

R = Read.

A0 = RDAC subaddress select bit.

SD = Shutdown connects wiper to B terminal and open circuits the A terminal. It does not change contents of wiper register.

T = OTP programming bit. Logic 1 programs the wiper permanently.

OW = Overwrites the fuse setting and program the digital potentiometer to a different setting. Upon power-up, the digital potentiometer is preset to either midscale or fuse setting, depending on whether or not the fuse link was blown.

D7, D6, D5, D4, D3, D2, D1, D0 = Data bits.

E1, E0 = OTP validation bits.

0, 0 = Ready to program.

1, 0 = Fatal error. Some fuses not blown. Do not retry. Discard this unit.

1, 1 = Programmed successfully. No further adjustments are possible.

**Table 9. Write Mode**

**AD5172**

| S | 0 | 1 | 0 | 1 | 1 | 1 | 1 | $\overline{W}$ | A | A0 | SD | T | 0 | OW | X | X | X | A | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | A | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Slave Address Byte | | | | | | | | | Instruction Byte | | | | | | | | | Data Byte | | | | | | | | | |

**AD5173**

| S | 0 | 1 | 0 | 1 | 1 | AD1 | AD0 | $\overline{W}$ | A | A0 | SD | T | 0 | OW | X | X | X | A | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | A | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Slave Address Byte | | | | | | | | | Instruction Byte | | | | | | | | | Data Byte | | | | | | | | | |

**Table 10. Read Mode**

**AD5172**

| S | 0 | 1 | 0 | 1 | 1 | 1 | 1 | R | A | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | A | E1 | E0 | X | X | X | X | X | X | A | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Slave Address Byte | | | | | | | | | Instruction Byte | | | | | | | | | Data Byte | | | | | | | | | |

**AD5173**

| S | 0 | 1 | 0 | 1 | 1 | AD1 | AD0 | R | A | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | A | E1 | E0 | X | X | X | X | X | X | A | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Slave Address Byte | | | | | | | | | Instruction Byte | | | | | | | | | Data Byte | | | | | | | | | |

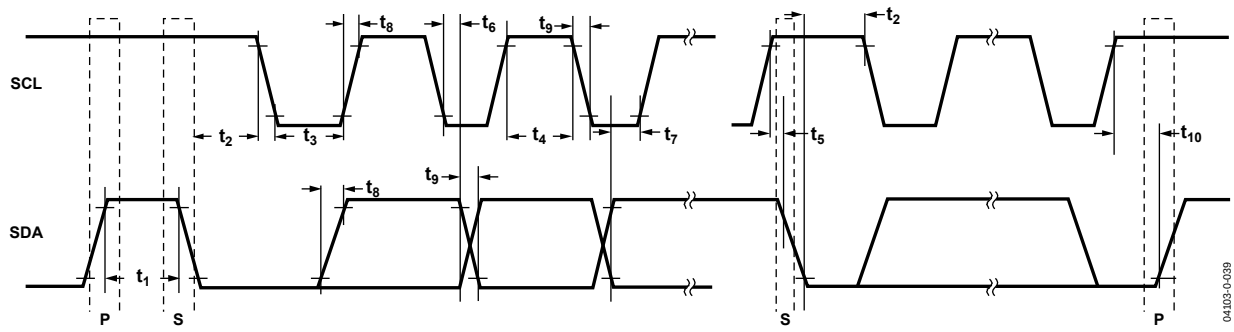



*Figure 51. I²C Interface Detailed Timing Diagram*

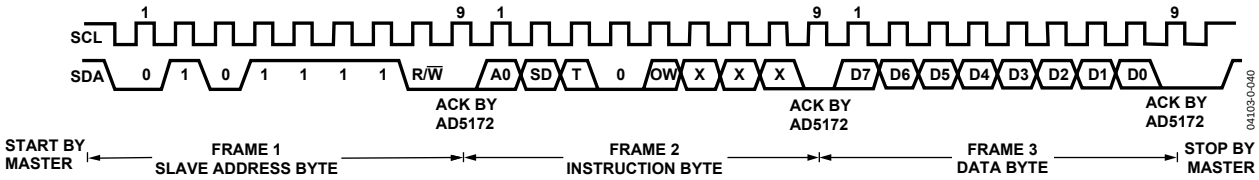



*Figure 52. Writing to the RDAC Register—AD5172*

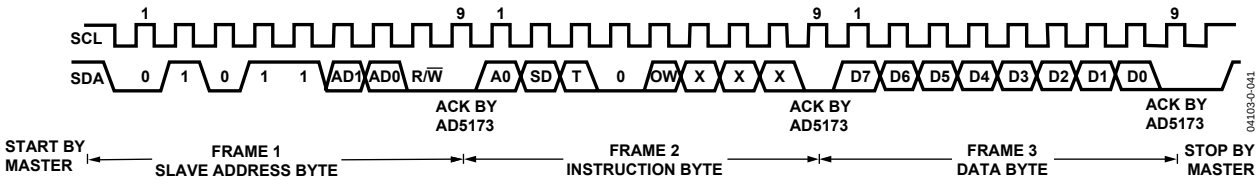



*Figure 53. Writing to the RDAC Register—AD5173*

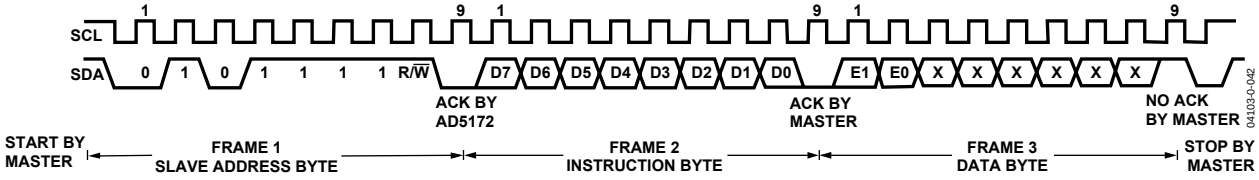



*Figure 54. Reading Data from a Previously Selected RDAC Register in Write Mode—AD5172*

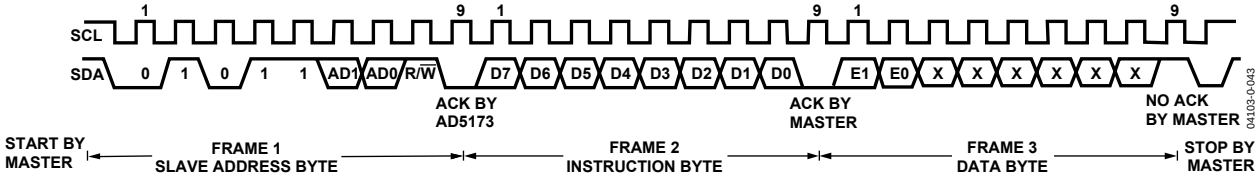



*Figure 55. Reading Data from a Previously Selected RDAC Register in Write Mode—AD5173*

## I²C-COMPATIBLE, 2-WIRE SERIAL BUS

This section describes how the 2-wire, I²C serial bus protocol operates.

The master initiates a data transfer by establishing a start condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 52 and Figure 53). The following byte is the slave address byte, which consists of the slave address followed by an R/$\overline{W}$ bit (this bit determines whether data is read from or written to the slave device). The AD5172 has a fixed slave address byte, whereas the AD5173 has two configurable address bits, AD0 and AD1 (see Figure 52 and Figure 53).

The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is called the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/$\overline{W}$ bit is high, the master reads from the slave device. If the R/$\overline{W}$ bit is low, the master writes to the slave device.

In write mode, the second byte is the instruction byte. The first bit (MSB) of the instruction byte is the RDAC subaddress select bit. Logic low selects Channel 1; logic high selects Channel 2.

The second MSB, SD, is a shutdown bit. A logic high causes an open circuit at Terminal A while shorting the wiper to Terminal B. This operation yields almost 0 Ω in rheostat mode or 0 V in potentiometer mode. It is important to note that the shutdown operation does not disturb the contents of the register. When brought out of shutdown, the previous setting is applied to the RDAC. In addition, during shutdown, new settings can be programmed. When the part is returned from shutdown, the corresponding VR setting is applied to the RDAC.

The third MSB, T, is the OTP programming bit. A logic high blows the polyfuses and programs the resistor setting permanently.

The fourth MSB must always be at Logic 0.

The fifth MSB, OW, is an overwrite bit. When raised to a logic high, OW allows the RDAC setting to be changed even after the internal fuses are blown. However, once OW is returned to Logic 0, the position of the RDAC returns to the setting prior to the overwrite. Because OW is not static, if the device is powered off and on, the RDAC presets to midscale or to the setting at which the fuses were blown, depending on whether or not the fuses were permanently set already.

The remainder of the bits in the instruction byte are don't cares (see Figure 52 and Figure 53).

After acknowledging the instruction byte, the last byte in write mode is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 51).

In read mode, the data byte follows immediately after the acknowledgment of the slave address byte. Data is transmitted over the serial bus in sequences of nine clock pulses (a slight difference from the write mode, where there are eight data bits followed by an acknowledge bit). Similarly, transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 54 and Figure 55).

Note that the channel of interest is the one that is previously selected in write mode. In the case where users need to read the RDAC values of both channels, they must program the first channel in the write mode and then change to read mode to read the first channel value. After that, the user must change back to write mode with the second channel selected and read the second channel value in read mode. It is not necessary for users to issue the Frame 3 data byte in write mode for subsequent readback operations. Refer to Figure 54 and Figure 55 for the programming format.

Following the data byte, the validation byte contains two validation bits, E0 and E1. These bits signify the status of the one-time programming (see Figure 54 and Figure 55).

**Table 11. Validation Status**

| E1 | E0 | Status |
|---|---|---|
| 0 | 0 | Ready for programming. |
| 1 | 0 | Fatal error. Some fuses not blown. Do not retry. Discard this unit. |
| 1 | 1 | Successful. No further programming is possible. |

After all data bits are read or written, a stop condition is established by the master. A stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition (see Figure 52 and Figure 53). In read mode, the master issues a No Acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master brings the SDA line low before the 10th clock pulse and then brings the SDA line high to establish a stop condition (see Figure 54 and Figure 55).

A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing and instructing the part only once. For example, after the RDAC has acknowledged its slave address and instruction bytes in write mode, the RDAC output is updated on each successive byte. If different instructions are needed, the write/read mode has to start again with a new slave address, instruction, and data byte. Similarly, a repeated read function of the RDAC is also allowed.

### *Multiple Devices on One Bus (AD5173 Only)*

Figure 56 shows four AD5173s on the same serial bus. Each has a different slave address because the states of their AD0 and AD1 pins are different. This allows each device on the bus to be written to or read from independently. The master device output bus line drivers are open-drain pull-downs in a fully I²C-compatible interface.

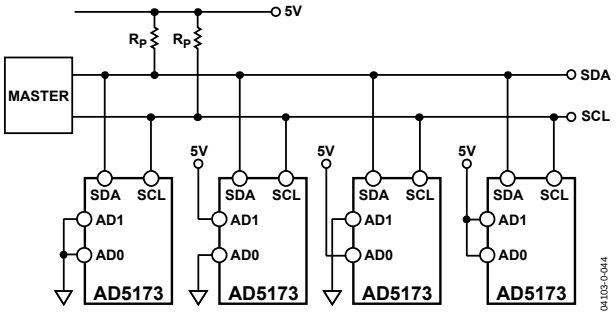



*Figure 56. Multiple AD5173s on One I²C Bus*

## LEVEL SHIFTING FOR DIFFERENT VOLTAGE OPERATION

If the SCL and SDA signals come from a low voltage logic controller and are below the minimum $V_{IH}$ level (0.7 V × $V_{DD}$), level shift the signals for read/write communications between the AD5172/AD5173 and the controller. Figure 57 shows one of the implementations. For example, when SDA1 is at 2.5 V, M1 turns off, and SDA2 becomes 5 V. When SDA1 is at 0 V, M1 turns on, and SDA2 approaches 0 V. As a result, proper level shifting is established. M1 and M2 should be low threshold N-channel power MOSFETs, such as FDV301N.

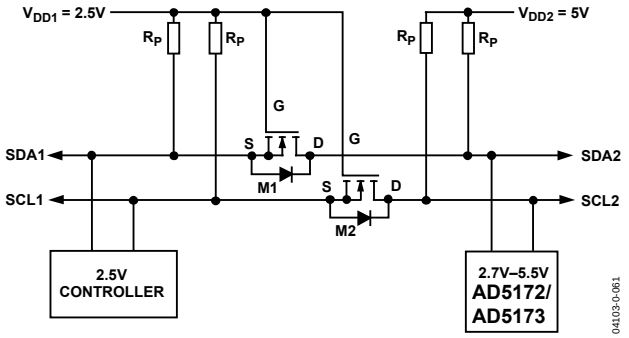
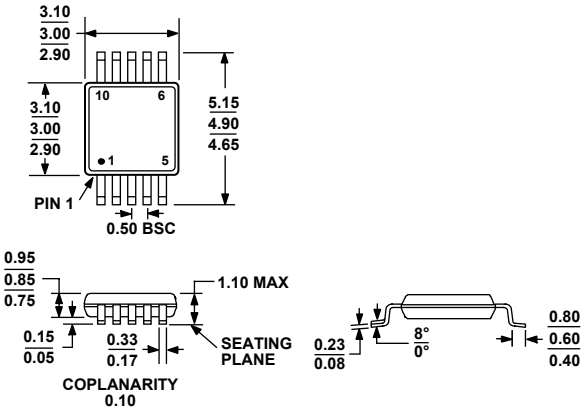



*Figure 57. Level Shifting for Different Voltage Operation*

# OUTLINE DIMENSIONS




**COMPLIANT TO JEDEC STANDARDS MO-187-BA**

*Figure 58. 10-Lead Mini Small Outline Package [MSOP]*
*(RM-10)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | $R_{AB}$ (kΩ) | Temperature Range | Package Description | Package Option | Branding |
|---|---|---|---|---|---|
| AD5172BRM2.5 | 2.5 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D0U |
| AD5172BRM2.5-RL7 | 2.5 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D0U |
| AD5172BRMZ2.5[2] | 2.5 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D0U# |
| AD5172BRM10 | 10 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D0V |
| AD5172BRM10-RL7 | 10 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D0V |
| AD5172BRMZ10[2] | 10 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D0V# |
| AD5172BRMZ10-RL7[2] | 10 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D0V# |
| AD5172BRM50 | 50 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D10 |
| AD5172BRM50-RL7 | 50 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D10 |
| AD5172BRMZ50[2] | 50 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D10# |
| AD5172BRMZ50-RL7[2] | 50 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D10# |
| AD5172BRM100 | 100 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D11 |
| AD5172BRM100-RL7 | 100 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D11 |
| AD5172BRMZ100[2] | 100 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D11# |
| AD5172BRMZ100-RL7[2] | 100 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D11# |
| AD5173BRM2.5 | 2.5 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D1K |
| AD5173BRM2.5-RL7 | 2.5 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D1K |
| AD5173BRMZ2.5[2] | 2.5 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D1K# |
| AD5173BRMZ2.5-RL7[2] | 2.5 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D1K# |
| AD5173BRM10 | 10 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D1L |
| AD5173BRM10-RL7 | 10 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D1L |
| AD5173BRMZ10[2] | 10 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D1L# |
| AD5173BRMZ10-RL7[2] | 10 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D1L# |
| AD5173BRM50 | 50 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D1M |
| AD5173BRM50-RL7 | 50 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D1M |
| AD5173BRMZ50[2] | 50 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D1M# |
| AD5173BRMZ50-RL7[2] | 50 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D1M# |
| AD5173BRM100 | 100 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D1N |
| AD5173BRM100-RL7 | 100 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D1N |
| AD5173BRMZ100[2] | 100 | –40°C to +125°C | 10-Lead MSOP | RM-10 | D1N# |

[1] The part has a YWW or #YWW label and an assembly lot number label on the bottom side of the package. The # stands for Pb-free part. The Y shows the year that the part is made; for example, Y = 5 means the part was made in 2005. WW shows the work week that the part is made.
[2] Z = Pb-free part, # denotes lead-free product may be top or bottom marked.

## NOTES

## NOTES

# NOTES

Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.


C04103-0-6/06(D)